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APPLICATION FOR PATENT

FOR INVENTION OF

QUASI-FEEDFORWARD PWM MODULATOR

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QUASI-FEEDFORWARD PWM MODULATOR

1. Field of the invention.

The present invention is related to the field of electric circuits, and more specifically to voltage dc to dc converters.

2. Background.

It is often desired to generate a voltage of a particular value, such as for use within a circuit. A converter may be used for this purpose, receiving a Direct Current (DC) input voltage, and outputting a DC voltage at the desired level. The input DC voltage, however, sometimes changes value, and it becomes necessary to adjust the converter to maintain the output voltage substantially constant.

Traditionally a converter was made from a voltage regulator that uses feedback. In other words, the output voltage is sensed ("fed back"), and then used to control the regulator. In a particular type of application, the regulator is a switching regulator, and control is by modulating the width of pulses ("pulse width modulation", or "PWM").

Another technique that has proven very useful in voltage mode pwm controllers is feedforward, which senses the input voltage in addition to the output voltage. The pwm ramp is modified according to the sensed input voltage – for example a peak to peak voltage is increased as the input voltage increases. A disadvantage of the feedforward topology is the required sensing of the input voltage. Another disadvantage is that the pwm ramp becomes vulnerable to noise on the input voltage, which requires some filtering to overcome.

In a voltage mode architecture, the cascade connection of the pwm modulator and the control to output transfer function are sometimes referred to as the plant (the object to be compensated). In some instances the gain of the plant is directly proportional to the input voltage. A problem has been when it is desired to compensate the transfer function to have enough phase margin for the highest input voltage case, because that causes the performance to suffer at the lowest input voltage case. The feedforward technique has

solved the problem by having an adjustable modulator gain inversely proportional to the input voltage, thus rendering the compensation of the transfer function independent from the input voltage. Nevertheless, that is a complex solution.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will become more readily apparent from the following Detailed Description, which proceeds with reference to the accompanying drawings, in which:

FIGURE 1 is a block diagram of a quasi-feedforward DC to DC converter circuit with substantially constant output voltage;

FIGURE 2 is a time plot of various waveforms of the circuit of FIGURE 1;

FIGURE 3A is a partial schematic for a sample buck configuration of a power storage element of FIGURE 1;

FIGURE 3B is a partial schematic for a sample boost configuration of a power storage element of FIGURE 1;

FIGURE 4 is a schematic diagram of a converter;

FIGURE 5 represents graphed plots of the output voltages resulting from the converter of FIGURE 4, by implementing the buck and boost configurations of FIGURES 3A and 3B; and

FIGURE 6 is a diagram illustrating a method according to an embodiment of the present invention.

DETAILED DESCRIPTION

The present invention is now described. While it is disclosed in its preferred form, the specific embodiments of the invention as disclosed herein and illustrated in the drawings are not to be considered in a limiting sense. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. Indeed, it should be readily apparent in view of the present description that the invention may be modified in numerous ways. Among other things, the present invention may be embodied as devices, methods, software, and so on. Accordingly, the present invention may take the form of an entirely hardware embodiment, an entirely software embodiment or an embodiment combining

software and hardware aspects. The following detailed description is, therefore, not to be taken in a limiting sense.

Throughout the specification, the meaning of "a," "an," and "the" may also include plural references. The meaning of "in" includes "in" and "on."

Briefly, the present invention provides devices, circuits and methods for generating a substantially constant output voltage. A power storage element generates a DC output voltage from an input voltage. An error amplifier generates an error signal from the output voltage and a reference voltage. In some embodiments, the output is sampled to generate a feedback signal, and the feedback signal is used by the error amplifier. A comparator generates a pulse signal by comparing a ramp signal and a compared voltage, where one of the ramp signal and the compared voltage is generated from the error signal. In some embodiments, the compared voltage is a preset threshold voltage, and the ramp signal is generated from the error signal. The resulting pulse signal is used to control a power switch, which switches the power storage element on and off. The pulse signal is generated such that, if the input voltage changes within a certain range, a width of its pulses changes so as to maintain the output voltage substantially constant.

The invention implements a modulator of the duty cycle of the pulse signal that has a small-signal gain inversely proportional to the input voltage. This maintains the loop gain substantially constant, in spite of any variations in the input voltage, which in turn maintains the output voltage substantially constant, in a way similar to feedforward topologies. The result is an improved input voltage step response, and better immunity to input voltage noise. As such, the invention is particularly suitable to generate the output voltage where a voltage is needed to be substantially constant.

The invention is now described in more detail.

FIGURE 1 is a block diagram of a quasi-feedforward converter 100 constructed according to the invention. Power storage element 110 receives a DC input voltage VIN, and generates a DC output voltage VOUT based at least in part on input voltage VIN. Output sampler 120 generates a feedback signal VF based at least in part on output voltage VOUT. Error amplifier 130 generates an error signal ER based on a preset reference voltage VREF and the feedback signal VF. Comparator 150 generates a pulse

signal VP based on a comparison of a ramp signal VR and a compared voltage. At least one of the ramp signal and the compared voltage is generated from the error signal ER. In the embodiment shown in FIGURE 1, the compared voltage is represented by a threshold voltage VT, and ramp generator 140 generates ramp signal VR based on at least the error signal. In one embodiment, ramp generator 140 and comparator 150 are reset by the same clock signal VCL. Power switch 160 switches power storage element 110 on and off. Power switch 160 is controlled by pulse signal VP for charging and discharging power storage element 110.

In one embodiment of converter 100, pulse signal VP is generated such that, if input voltage VIN changes within a first range, the width of the pulses of the pulse signal is adjusted to maintain output voltage VOUT substantially constant. This type of adjustment is called Pulse Width Modulation (PWM).

FIGURE 2 illustrates time plots of various waveforms for circuit 100. Input voltage VIN has a sample waveform 210, which undergoes a change. At a first segment 212 input voltage VIN is of a high value, at a second segment 214 it decreases, and at a third segment 216 it maintains a low value. These segments could represent for example, a voltage change from 9V to 3V, in other words a voltage swing within a relatively substantial range.

Clock signal VCL has a waveform 220, with optimally periodic pulses. Threshold voltage VT has a waveform 230 that is relatively constant.

Ramp signal VR has a waveform 240. As shown, ramp signal VR is reset by clock pulse VCL, and starts increasing. It continues increasing until it reaches threshold voltage VT, and stops increasing shortly after that. As will be seen later, the rising line has a slope that can change. Then the voltage of ramp signal VR remains substantially constant, until it is reset by the next clock pulse of clock signal VCL.

Pulse signal VP has a waveform 250 that moves from zero to one on the falling edge of a pulse of clock signal VCL. Then it moves to zero again, when ramp signal VR reaches threshold voltage VT. Accordingly, the pulses of pulse signal VP have a period that is substantially constant, and depends on the period of clock signal VCL. Also the width of pulses in pulse signal VP depends at least in part on how fast ramp signal VR is increasing at the moment.

During first segment 212, input voltage VIN is constant. Accordingly, the slope of the rising line of ramp signal VR is substantially the same for every ramp. Therefore, the corresponding pulses of pulse signal VP have substantially the same width.

During second segment 214, input voltage VIN is decreasing. Accordingly, the slope of the rising line of ramp signal VR diminishes with every new ramp. Therefore, the corresponding pulses of pulse signal VP have increasing widths relative to each other.

During third segment 216, input voltage VIN is constant, but at a value lower than that of first segment 212. Accordingly, the slope of the rising line of ramp signal VR is substantially the same for every ramp (but lower than in the previous ramps). Therefore, the corresponding pulses of pulse signal VP have substantially the same width as each other (but larger than the width of the previous pulses).

In all of these cases, the slope varies substantially inversely to the duty cycle. Generally, the duty cycle may be given by the ratio of VOUT/VIN. In that case, the slope varies as the inverse of VIN, if VOUT is to be maintained substantially constant.

As discussed above, when input voltage VIN changed through three segments 212, 214, 216 of differing values, the width of the pulses of pulse signal VP also changed. This change is a form of Pulse Width Modulation (PWM) that compensates for changes in the value of input voltage VIN. Accordingly, output signal VOUT (waveform 260) is maintained at a substantially constant value.

Returning to FIGURE 1, power storage element 110 may be implemented in a number of configurations, to construct different types of converters. These configurations include but are not limited to buck, boost, cuk, sepic and zeta. Of those, the invention works better with a buck configuration than a boost configuration. The buck and boost configuration are described below in more detail.

FIGURE 3A illustrates a partial schematic 320 for a sample buck configuration. In a buck configuration, output voltage VOUT is less than input voltage VIN. A power storage element is provided, such as inductor 330. Charging inductor 330 is controlled by power switch 360. A capacitor is provided, than can be charged by inductor 330. A diode is provided that prevents the capacitor from discharging to ground.

In a charging phase, switch 360 is closed, and the capacitor is charged through inductor 330. The current through inductor 330 starts increasing, but it cannot change

instantaneously from its previous value. Inductor 330 maintains a substantially constant voltage across it, which is subtracted from input voltage VIN to define output voltage VOUT.

In a discharging phase, switch 360 is opened. However, the current through inductor 330 cannot change instantaneously, so inductor 330 draws current through the diode, albeit at a decreasing rate, to maintain output voltage VOUT across the capacitor substantially constant.

FIGURE 3B illustrates a partial schematic 380 for a sample boost configuration. In a boost configuration, output voltage VOUT is larger than input voltage VIN. A power storage element is provided, such as inductor 390. Charging inductor 390 is controlled by power switch 360. A capacitor is provided, than can be charged by inductor 390. A diode is also provided that prevents the capacitor from discharging to ground.

In a charging phase, switch 360 is closed from the open position. The current through inductor 390 starts increasing. However, since this current cannot change instantaneously from its previous value, output voltage VOUT is maintained at a substantially constant value.

In a discharging phase, switch 360 is opened from the closed position. The current through inductor 390 starts decreasing, but it cannot change instantaneously from its previous value. However, all of it is used to maintain the capacitor charged, which maintains output voltage VOUT at a substantially constant value.

FIGURE 4 shows a partial schematic of a quasi-feedforward converter 400 for receiving input voltage VIN, and generating output voltage VOUT. It will be recognized that converter 400 has many elements similar to converter 100. Power storage element 410 may include an inductor. An output sampler is implemented by two resistors 420 to generate a feedback voltage VF. Resistors 420 implement an impedance divider. Error amplifier 430 generates error signal ER from feedback voltage VF and from reference voltage VREF. Additionally, other elements such as a capacitor resistor network may be added between error signal ER and feedback voltage VF, to control the frequency response of converter 400.

Ramp generator 440 generates ramp signal VR from error signal ER. In the embodiment shown in FIGURE 4, ramp generator 440 includes ramp capacitor 442, and ramp switch 444 to charge ramp capacitor 442 in accordance with error signal ER. Ramp generator 440 further includes reset switch 446 to short ramp capacitor 444, upon reset. Reset may occur from a pulse of clock signal VCL. Ramp generator 440 additionally includes a linear element to control charging of ramp capacitor 442 through ramp switch 444. In the embodiment shown in FIGURE 4, the linear element is represented by resistor 448, also known as a degeneration resistor in this case.

Comparator 450 compares ramp signal VR with a threshold voltage VT, and accordingly generates pulse signal VP. A power switch is implemented by a MOSFET 460. Element 410 and transistor 460 may be configured as shown in FIGURE 3A or FIGURE 3B, such as for power switch 360. A gate of transistor 460 receives pulses from pulse signal VP, and accordingly switches on and off power storage element 410.

FIGURE 5 represents graphed plots of output voltages VOUT as a function of input voltages VIN resulting from a converter according to the invention, such as converters 100, 400. When the buck configuration 320 of FIGURE 3A is implemented, the result is plot 520. When the boost configuration 380 of FIGURE 3A is implemented, the result is plot 580.

FIGURE 6 shows a diagram 600 for illustrating a method according to an embodiment of the invention. The method of diagram 600 may also be practiced by different embodiments of the invention, including but not limited to circuits 100 and 400.

The blocks of diagram 600 are interrelated as shown. Starting at block 610, there is charging and discharging of a power element to generate an output voltage. At optional next block 620, the output voltage is sampled to generate a feedback signal. At next block 630, an error signal is generated from the output voltage. If optional block 620 is indeed implemented, then the error signal is generated from the feedback signal. At next block 640, a ramp signal is generated from the error signal. At next block 650, the ramp signal is compared to a preset threshold voltage, which facilitates the generation of a pulse signal. At next block 660, the pulse signal is used to control the alternating charging and discharging of block 610.

Numerous details have been set forth in this description, which is to be taken as a whole, to provide a more thorough understanding of the invention. In other instances, well-known features have not been described in detail, so as to not obscure unnecessarily the invention.

The invention includes combinations and subcombinations of the various elements, features, functions and/or properties disclosed herein. The following claims define certain combinations and subcombinations, which are regarded as novel and non-obvious. Additional claims for other combinations and subcombinations of features, functions, elements and/or properties may be presented in this or a related document.